WHAT IS CLAIMED IS:

1. A method comprising:

a transmitting device transmitting data at a first non-zero rate to a memory for storage therein during a first period of time;

the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time;

wherein the second period of time is subsequent to the first period of time, and;

wherein the second non-zero rate is greater than or less than the first non-zero rate.

2. The method of claim 1 wherein the memory device comprises a FIFO buffer:

3. The method of claim 1 wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

4. The method of claim 1 further comprising:

generating a rate control signal to the transmitting device instructing the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate;

transmitting the rate control signal to the transmitting device;

wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal.

5. The method of claim 4 further comprising:

generating first data quantity value representing a quantity of data stored in the memory device at a first point in time;

comparing the first data quantity value to a first predetermined value;

wherein the rate control signal is generated in response to comparing the first data quantity value to the first predetermined value.

6. The method of claim 5 further comprising:

comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values;

wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values.

7. The method of claim 5 further comprising:

generating second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time;

comparing the first data quantity value to the second data quantity value;

wherein the rate control signal is generated if the first data quantity value is not equal to the second data quantity value.

8. The method of claim 5 wherein generating the first data quantity value comprises:

generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time;

generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time;

subtracting the total data output count from total data input count.

9. The method of claim 7 wherein the second non-zero rate is greater than the first non-zero rate if the second data quantity value is less than the first data quantity value, and wherein the second non-zero rate is less than the first non-zero rate if the second data quantity value is less than the first data quantity value.

10. An apparatus comprising:

a memory device configured to receive data from a transmitting device for storage therein;

a circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate;

wherein the second non-zero rate is greater than or less than the first non-zero rate.

11. The apparatus of claim 10 wherein the memory device comprises a FIFO buffer.

12. The apparatus of claim 10 further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

13. The apparatus of claim 10 further comprising:

a first circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time;

a first comparing circuit for comparing the first data quantity value to a first predetermined value;

wherein the circuit generates the rate control signal in response to comparing the first data quantity value to the first predetermined value.

14. The apparatus of claim 13 further comprising:

a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values, wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values;